ABSTRACT

A method of overerase correction for memory cells in a memory array after the memory cells have been erased is provided comprising the following steps: (a) setting a gate voltage of memory cells from a first selected bit line exhibiting leakage current above a threshold value to an initial voltage level; (b) applying a series of overerase correction pulses to the first selected bit line during a selected time period; (c) detecting during the selected time period whether the bit line exhibits leakage current above the threshold value; (d) if the bit line exhibits leakage current above the threshold value after the selected time period, increasing the gate voltage and repeating steps (b) and (c); and (e) if it is detected that the bit line does not exhibit leakage current above the threshold value during the selected time period, selecting a second bit line and repeating steps (a) through (d).